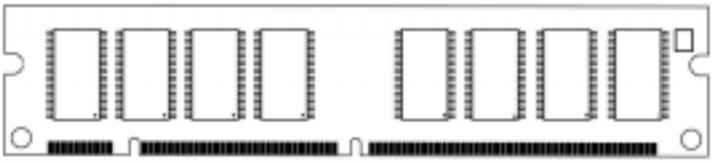
MACROTRON

MS3328L3264S-07

256MB SDRAM DIMM

32Mb x 64, 168-Pin DIMM
3.3V Synchronous DRAMs with SPD

FRONT VIEW



BACK VIEW

GENERAL DESCRIPTION

The Macrotron MS3328L3264S-07 is a PC133 Compliant 32M bit x 64 bit Synchronous Dynamic RAM high density memory module. It consists of eight CMOS 32M x 8 bit with Synchronous DRAMs in TSOP packages and a 2K EEPROM in 8-pin TSOP package on a 168-pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The product is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle controls with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- 32 Megabit by 64 bit (256 Megabyte) Synchronous DRAM Module PC 133 Compliant
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 7.5ns SDRAM components
- Nonbuffered
- Single +3.3V $\pm$ 0.3V power supply
- Fully synchronous; all signals registered on positive edge system clock
- Internal pipeline operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge
- Programmable burst lengths: 1,2,4 or 8
- Auto Precharged and Auto Refresh Modes
- LVTTL compatible inputs and outputs
- Serial Presence Detect (SPD)

PART NUMBER DESIGNATOR

MS 3 328 L 3264 S -07

- -07 — Module Speed (uses 7.5ns DRAMS)
- S — Synchronous
- 3264 — Module Configuration of 32Mb x 64 bit
- L — PCB Revision Level L
- 328 — SDRAM Configuration of 32Mb x 8 bit
- 3 — 168-Pin DIMM
- MS — Macrotron Systems

KEY TIMING PARAMETERS

PARAMETER	VALUE	UNIT
Module Bus Speed	133	MHz
Module Speed	7.5	ns
SDRAM Speed	133	MHz
CAS Latency	2/3	CLOCK
SDRAM Access Time	5.4	ns
SDRAM Setup Time	1.5	ns
SDRAM Hold Time	0.8	ns

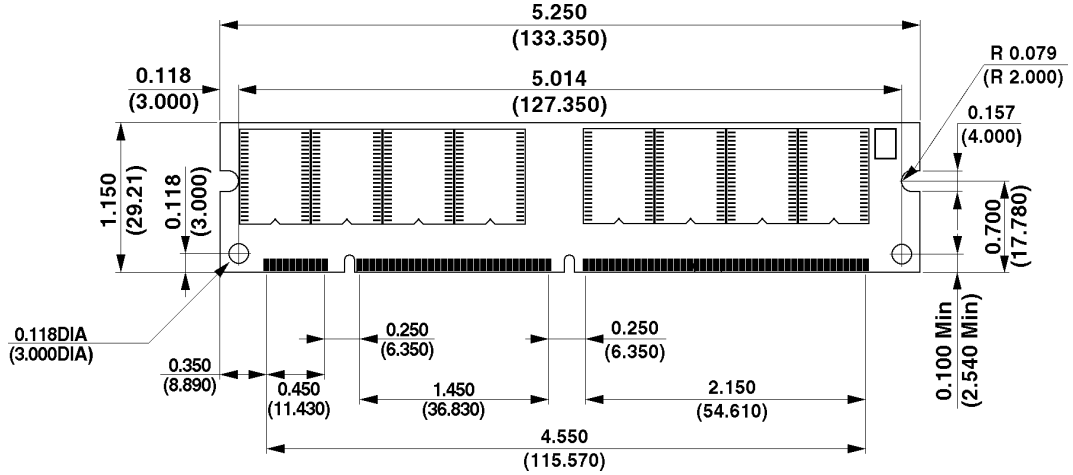
PIN CONFIGURATIONS

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	29	DQMB1	57	DQ18	85	VSS	113	DQMB5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQMB2	74	DQ28	102	VDD	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CBO	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQMB0	56	DQ17	84	VDD	112	DQMB4	140	DQ49	168	VDD

PIN NAMES

PIN NAME	FUNCTION
A0~A13	Address Input (multiplexed)
BA0~BA1	Select Bank
DQ0~DQ63	Data Input / Data Output
CLK0~CLK3	Clock Input
CKE0~CKE1	Clock Enable Input
CS0~CS3	Chip Select Input
RAS	Row Address Storbe
CAS	Column Address Storbe
WE	Write Enable
DQMB0~7	DQMB
VDD	Power Supply (3.3V)
VSS	Ground
VREF	Power Supply for Reference
SDA	Serial Data I/O
SCL	Serial Clock
SA0~2	Address in EEPROM
DU	Don't Use
NC	No Connection
AP	Automatic Precharge
WP	Write Protection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	VALUE	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	C
Power Dissipation	PD	8	W
Short Circuit Current	I_{OS}	50	mA

DC OPERATING CONDITIONS AND CHARACTERISTICS

PARAMETERS		SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage		V_{DD}	3.0	3.6	V	
Input High Voltage (Logic 1), All Inputs		V_{IH}	2.0	V_{DD} + 0.3	V	
Input low Voltage (Logic 0), All Inputs		V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT	DQMB0~DQMB7	I_{I1}	-10	10	µA	
Any input 0V $\leq V_{IN} \leq V_{DD}$	CLK0~2, CS0~2#	I_{I2}	-10	10	µA	
(All other pins not under test = 0V)	CKE0~1	I_{I3}	-10	10	µA	
	RAS, CAS, A0~A11, BA0~1, WE	I_{I4}	-10	10	µA	
OUTPUT LEAKAGE CURRENT	DQ0~DQ63	I_{OZ}	-10	10	µA	
(DQs are disabled; 0V $\leq V_{OUT} \leq V_{DD}$						
OUTPUT LEVELS						
Output High Voltage		V_{OH}	2.4			I_{OH} = -2mA
Output low Voltage		V_{OL}		0.4	V	I_{OL} = 2mA

CAPACITANCE (V_{DD} = 3.3V, TA = 23C, F = 1MHZ, VREF = 1.4V)

PARAMETERS	SYMBOL	MAX	UNIT
Input Capacitance (A_0 ~ A_n, BA0~1, RAS, CAS, WE)	C_{I1}	28	pF
Input Capacitance (CS0~2#)	C_{I2}	20	pF
Input Capacitance (CKE0~1)	C_{I3}	35	pF
Input Capacitance (DQMB0~7)	C_{I4}	7	pF
Input Capacitance (SCL, SA0-2, WP)	C_{I5}	6	pF
Data Input/Output Capacitance (DQ0~63, SDA)	C_{I0}	8	pF
Input Capacitance (CLK0~3)	C_{I6}	15	pF

OPERATING CONDITIONS AND MAXIMUM LIMITS

PARAMETER/CONDITION	SYMBOL	MAX	UNITS
OPERATING CURRENT: Active Mode, Burst =2 READ or WRITE, tRC ≥ tRC (MIN), CAS Latency = 3	ICC1	1280	mA
STANDBY CURRENT: Power-Down Mode, tCK = 7.5ns, CKE ≤ V_{IL} (MAX), All banks idle	ICC2	16	mA
STANDBY CURRENT: CS ≥ V_{IH} (MIN), tCK = 7.5ns, CKE ≥ V_{IH} (MAX), All banks idle	ICC3	48	mA
STANDBY CURRENT: CS ≥ V_{IH} (MIN) tCK = 7.5ns, CKE ≥ V_{IH} (MIN), all banks active after tRCD met, No accesses in progress	ICC4	700	mA
OPERATING CURRENT: Burst Mode, Continuous burst, READ or WRITE, tCK = 7.5ns, all banks active, Addresses transition once per clock cycle, CAS Latency = 3	ICC5	1240	mA
AUTO REFRESH CURRENT: tRC ≥ tRC (MIN), CAS Latency = 3	ICC6	2080	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	ICC7	40	mA

AC FUNCTIONAL CHARACTERISTICS

PARAMETERS		SYMBOL		UNITS
READ/WRITE command to READ/WRITE command		tCCD	1	tCK
CKE to clock disable or power-down entry mode		tCKED	1	tCK
CKE to clock enable or power-down exit mode		tPED	1	tCK
DQM to input data delay		tDQD	0	tCK
DQM to data mask during WRITEs		tDQM	0	tCK
DQM to data high-impedance during READs		tDQZ	2	tCK
WRITE command to input data delay		tDWD	0	tCK
Data-in to PRECHARGE command		tDAL	2	tCK
Data-in to ACTIVE command		tDPL	5	tCK
Last data-in to PRECHARGE command		tRDL	2	tCK
Last data-in to burst STOP command		tBDL	1	tCK
Last data-in to new READ/WRITE command		tCDL	1	tCK
LOAD MODE REGISTER command to command		tMRD	2	tCK
Data-out to high-impedance from PRECHARGE command	CAS latency=3	tROH	3	tCK
	CAS latency=2	tROH	2	tCK

FUNCTIONAL BLOCK DIAGRAM