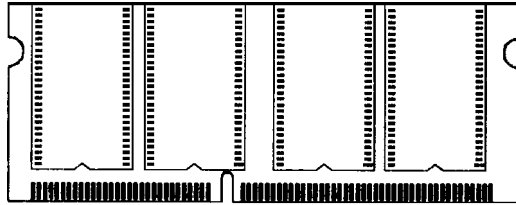
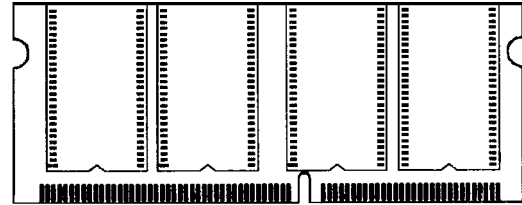


FRONT VIEW



BACK VIEW



## GENERAL DESCRIPTION

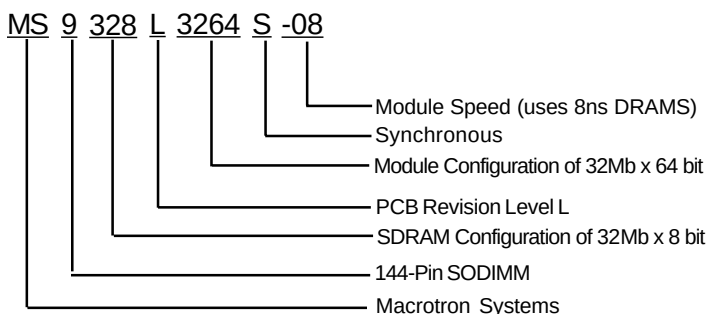
The Macrotron MS9328L3264S-08 is a PC100 Compliant 32M bit x 64 bit Synchronous Dynamic RAM high density memory module. It consists of eight CMOS 32M x 8 bit Synchronous DRAMs in TSOP packages and a 2K EEPROM in 8-pin TSOP package on a 144-pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The product is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle controls with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

## FEATURES

- 32 Megabit by 64 bit (256 Megabyte) Synchronous DRAM Module PC 100 Compliant
- JEDEC-standard 144-pin small outline, dual in-line memory module (SODIMM)
- Utilizes 8ns SDRAM components
- Nonbuffered
- Single +3.3V  $\pm$  0.3V power supply
- Fully synchronous; all signals registered on positive edge system clock
- Internal pipeline operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge
- Programmable burst lengths: 1,2,4, or 8
- Auto Precharged and Auto Refresh Modes
- LVTTTL compatible inputs and outputs
- Serial Presence Detect (SPD)

## PART NUMBER DESIGNATOR



## KEY TIMING PARAMETERS

| PARAMETER         | VALUE | UNIT  |
|-------------------|-------|-------|
| Module Bus Speed  | 100   | MHz   |
| Module Speed      | 8.0   | ns    |
| SDRAM Speed       | 125   | MHz   |
| CAS Latency       | 2/3   | CLOCK |
| SDRAM Access Time | 6.0   | ns    |
| SDRAM Setup Time  | 2.0   | ns    |
| SDRAM Hold Time   | 1.0   | ns    |

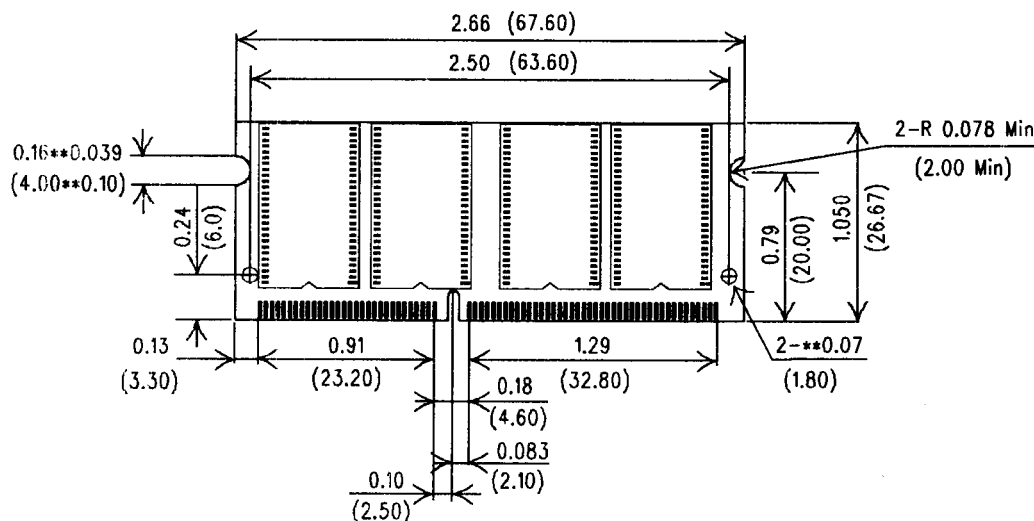
### PIN CONFIGURATIONS

| PIN | FRONT | PIN | BACK | PIN | FRONT | PIN | BACK | PIN | FRONT  | PIN | BACK  |
|-----|-------|-----|------|-----|-------|-----|------|-----|--------|-----|-------|
| 1   | VSS   | 2   | VSS  | 51  | DQ14  | 52  | DQ46 | 101 | VDD    | 102 | VDD   |
| 3   | DQ0   | 4   | DQ32 | 53  | DQ15  | 54  | DQ47 | 103 | A6     | 104 | A7    |
| 5   | DQ1   | 6   | DQ33 | 55  | VSS   | 56  | VSS  | 105 | A8     | 106 | BA0   |
| 7   | DQ2   | 8   | DQ34 | 57  | NC    | 58  | NC   | 107 | VSS    | 108 | VSS   |
| 9   | DQ3   | 10  | DQ35 | 59  | NC    | 60  | NC   | 109 | A9     | 110 | BA1   |
| 11  | VDD   | 12  | VDD  | 61  | CLK0  | 62  | CKE0 | 111 | A10/AP | 112 | A11   |
| 13  | DQ4   | 14  | DQ36 | 63  | VDD   | 64  | VDD  | 113 | VDD    | 114 | VDD   |
| 15  | DQ5   | 16  | DQ37 | 65  | RAS   | 66  | CAS  | 115 | DQM2   | 116 | DQM6  |
| 17  | DQ6   | 18  | DQ38 | 67  | WE    | 68  | CKE1 | 117 | DQM3   | 118 | DQM7  |
| 19  | DQ7   | 20  | DQ39 | 69  | CS0   | 70  | *A12 | 119 | VSS    | 120 | VSS   |
| 21  | VSS   | 22  | VSS  | 71  | CS1   | 72  | *A13 | 121 | DQ24   | 122 | DQ56  |
| 23  | DQM0  | 24  | DQM4 | 73  | DU    | 74  | CLK1 | 123 | DQ25   | 124 | DQ57  |
| 25  | DQM1  | 26  | DQM5 | 75  | VSS   | 76  | VSS  | 125 | DQ26   | 126 | DQ58  |
| 27  | VDD   | 28  | VDD  | 77  | NC    | 78  | NC   | 127 | DQ27   | 128 | DQ59  |
| 29  | A0    | 30  | A3   | 79  | NC    | 80  | NC   | 129 | VDD    | 130 | VDD   |
| 31  | A1    | 32  | A4   | 81  | VDD   | 82  | VDD  | 131 | DQ28   | 132 | DQ60  |
| 33  | A2    | 34  | A5   | 83  | DQ16  | 84  | DQ48 | 133 | DQ29   | 134 | DQ61  |
| 35  | VSS   | 36  | VSS  | 85  | DQ17  | 86  | DQ49 | 135 | DQ30   | 136 | DQ62  |
| 37  | DQ8   | 38  | DQ40 | 87  | DQ18  | 88  | DQ50 | 137 | DQ31   | 138 | DQ63  |
| 39  | DQ9   | 40  | DQ41 | 89  | DQ19  | 90  | DQ51 | 139 | VSS    | 140 | VSS   |
| 41  | DQ10  | 42  | DQ42 | 91  | VSS   | 92  | VSS  | 141 | **SDA  | 142 | **SCL |
| 43  | DQ11  | 44  | DQ43 | 93  | DQ20  | 94  | DQ52 | 143 | VDD    | 144 | VDD   |
| 45  | VDD   | 46  | VDD  | 95  | DQ21  | 96  | DQ53 |     |        |     |       |
| 47  | DQ12  | 48  | DQ44 | 97  | DQ22  | 98  | DQ54 |     |        |     |       |
| 49  | DQ13  | 50  | DQ45 | 99  | DQ23  | 100 | DQ55 |     |        |     |       |

\* These pins are not used in this module.  
\*\* These pins should be NC in the system which does not support SPD

### PIN NAMES

| PIN NAME  | FUNCTION                    |
|-----------|-----------------------------|
| A0~An     | Address Input (multiplexed) |
| BA0~BA1   | Select Bank                 |
| DQ0~DQ63  | Data Input / Data Output    |
| CLK0~CLK1 | Clock Input                 |
| CKE0~CKE1 | Clock Enable Input          |
| CS0~CS1   | Chip Select Input           |
| RAS       | Row Address Strobe          |
| CAS       | Column Address Strobe       |
| WE        | Write Enable                |
| DQM0~7    | DQM                         |
| VDD       | Power Supply (3.3V)         |
| VSS       | Ground                      |
| SDA       | Serial Data I/O             |
| SCL       | Serial Clock                |
| DU        | Don't Use                   |
| NC        | No Connection               |



**ABSOLUTE MAXIMUM RATINGS**

| PARAMETERS                                      | SYMBOL            | VALUE      | UNIT |
|-------------------------------------------------|-------------------|------------|------|
| Voltage on any pin relative to $V_{SS}$         | $V_{IN}, V_{OUT}$ | -1.0 ~ 4.6 | V    |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}, V_{DDQ}$ | -1.0 ~ 4.6 | V    |
| Storage Temperature                             | $T_{STG}$         | -55 ~ +150 | C    |
| Power Dissipation                               | PD                | 8          | W    |
| Short Circuit Current                           | $I_{OS}$          | 50         | mA   |

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

| PARAMETERS                                                                                              |                           | SYMBOL   | MIN  | MAX            | UNIT    | NOTES           |
|---------------------------------------------------------------------------------------------------------|---------------------------|----------|------|----------------|---------|-----------------|
| Supply Voltage                                                                                          |                           | $V_{DD}$ | 3.0  | 3.6            | V       |                 |
| Input High Voltage (Logic 1), All Inputs                                                                |                           | $V_{IH}$ | 2.0  | $V_{DD} + 0.3$ | V       |                 |
| Input low Voltage (Logic 0), All Inputs                                                                 |                           | $V_{IL}$ | -0.5 | 0.8            | V       |                 |
| INPUT LEAKAGE CURRENT<br>Any input $0V \leq V_{IN} \leq V_{DD}$<br>(All other pins not under test = 0V) | DQMB0~7                   | $I_{I1}$ | -10  | 10             | $\mu A$ |                 |
|                                                                                                         | CK0~3, CS0~3#             | $I_{I2}$ | -20  | 20             | $\mu A$ |                 |
|                                                                                                         | CKE0~1                    | $I_{I3}$ | -40  | 40             | $\mu A$ |                 |
|                                                                                                         | RAS, CAS, A0~A11, BA0, WE | $I_{I4}$ | -80  | 80             | $\mu A$ |                 |
| OUTPUT LEAKAGE CURRENT<br>(DQs are disabled; $0V \leq V_{OUT} \leq V_{DD}$ )                            |                           | $I_{OZ}$ | -10  | 10             | $\mu A$ |                 |
| OUTPUT LEVELS                                                                                           |                           |          |      |                |         |                 |
| Output High Voltage                                                                                     |                           | $V_{OH}$ | 2.4  |                | V       | $I_{OH} = -2mA$ |
| Output low Voltage                                                                                      |                           | $V_{OL}$ |      | 0.4            | V       | $I_{OL} = 2mA$  |

**CAPACITANCE** ( $V_{DD} = 3.3V$ ,  $T_A = 23C$ ,  $F = 1MHZ$ ,  $V_{REF} = 1.4V$ )

| PARAMETERS                                              | SYMBOL   | MAX | UNIT |
|---------------------------------------------------------|----------|-----|------|
| Input Capacitance ( $A_0 \sim A_n$ , BA0, RAS, CAS, WE) | $C_{I1}$ | 65  | pF   |
| Input Capacitance (CS0~3)                               | $C_{I2}$ | 24  | pF   |
| Input Capacitance (CKE0~1)                              | $C_{I3}$ | 45  | pF   |
| Input Capacitance (DQMB0~7)                             | $C_{I4}$ | 13  | pF   |
| Input Capacitance (SCL, SA0~2)                          | $C_{I5}$ | 6   | pF   |
| Data Input/Output Capacitance (DQ0~63, SDA)             | $C_{I0}$ | 15  | pF   |
| Input Capacitance (CK0~3)                               | $C_{I6}$ | 20  | pF   |

### OPERATING CONDITIONS AND MAXIMUM LIMITS

| PARAMETER/CONDITION                                                                                                                                                  | SYMBOL | MAX  | UNITS |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------|-------|
|                                                                                                                                                                      |        |      |       |
| OPERATING CURRENT: Active Mode, Burst =2<br>READ or WRITE, $t_{RC} \geq t_{RC} (MIN)$ , CAS Latency = 3                                                              | ICC1   | 1440 | mA    |
| STANDBY CURRENT: Power-Down Mode,<br>$t_{CK} = 10ns$ , $CKE \leq V_{IL} (MAX)$ , All banks idle                                                                      | ICC2   | 16   | mA    |
| STANDBY CURRENT: $CS \geq V_{IH} (MIN)$ ,<br>$t_{CK} = 10ns$ , $CKE \geq V_{IH} (MAX)$ , All banks idle                                                              | ICC3   | 48   | mA    |
| STANDBY CURRENT: $CS \geq V_{IH} (MIN)$<br>$t_{CK} = 10ns$ , $CKE \geq V_{IH} (MIN)$ , all banks<br>active after $t_{RCD}$ met, No accesses in progress              | ICC4   | 640  | mA    |
| OPERATING CURRENT: Burst Mode, Continuous burst,<br>READ or WRITE, $t_{CK} = 10ns$ , all banks active,<br>Addresses transition once per clock cycle, CAS Latency = 3 | ICC5   | 1440 | mA    |
| AUTO REFRESH CURRENT: $t_{RC} > t_{RC} (MIN)$ , CAS Latency = 3                                                                                                      | ICC6   | 2240 | mA    |
| SELF REFRESH CURRENT: $CKE \leq 0.2V$                                                                                                                                | ICC7   | 24   | mA    |

### AC FUNCTIONAL CHARACTERISTICS

| PARAMETERS                                        |               | SYMBOL     |   | UNITS |
|---------------------------------------------------|---------------|------------|---|-------|
| READ/WRITE command to READ/WRITE command          |               | $t_{CCD}$  | 1 | tCK   |
| CKE to clock disable or power-down entry mode     |               | $t_{CKED}$ | 1 | tCK   |
| CKE to clock enable or power-down exit mode       |               | $t_{PED}$  | 1 | tCK   |
| DQM to input data delay                           |               | $t_{DQD}$  | 0 | tCK   |
| DQM to data mask during WRITES                    |               | $t_{DQM}$  | 0 | tCK   |
| DQM to data high-impedance during READs           |               | $t_{DQZ}$  | 2 | tCK   |
| WRITE command to input data delay                 |               | $t_{DWD}$  | 0 | tCK   |
| Data-in to PRECHARGE command                      |               | $t_{DAL}$  | 2 | tCK   |
| Data-in to ACTIVE command                         |               | $t_{DPL}$  | 4 | tCK   |
| Last data-in to PRECHARGE command                 |               | $t_{RDL}$  | 2 | tCK   |
| Last data-in to burst STOP command                |               | $t_{BDL}$  | 1 | tCK   |
| Last data-in to new READ/WRITE command            |               | $t_{CDL}$  | 1 | tCK   |
| LOAD MODE REGISTER command to command             |               | $t_{MRD}$  | 2 | tCK   |
| Data-out to high-impedance from PRECHARGE command | CAS latency=3 | $t_{ROH}$  | 3 | tCK   |
|                                                   | CAS latency=2 | $t_{ROH}$  | 2 | tCK   |
|                                                   | CAS latency=1 | $t_{ROH}$  | 1 | tCK   |

### FUNCTIONAL BLOCK DIAGRAM

